

REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated October 22, 2004. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-3 are under consideration in this application. Claim 1 is being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicant's invention.

Additional Amendments

Claim 1 is being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 1-2 were rejected under 35 U.S.C. § 102(a)/102(e) on the grounds of being anticipated by US Pat. No. 6,339,560 to Naritake (hereinafter "Naritake"), and claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Naritake in view of US Pat. No. 5,506,808 to Yamada et al. (hereinafter "Yamada"). The prior art reference of Tomishima et al. (6,314,042) was cited as being pertinent to the present application. These rejections have been carefully considered, but are most respectfully traversed.

As now recited in claim 1, the read signal line (e.g., WIOT, WIOB in Fig. 1) is *different* from said write signal line according to the invention (e.g., RIOT, RIOB in Figs. 1, 6). A write operation is being executed at the same time (the timing overlapping of read operation in Fig. 4 with the write operation in Fig. 5; *"the column selection switch for read is turned ON even*

during the write operation” p. 2, lines 12-14) as a read operation form an Y/column address that is different from the Y/column address of the write operation (“the Y selection line WYS for write to control the operation of the column selection switch in the write amplifier is isolated from the Y selection line RYS for read to control the operation of the column selection switch in the read amplifier” p. 6, lines 10-12).

In contrast, Naritake reads and writes data on the *same* pair of data lines DLn, /DLn (Fig. 2; col. 4, lines 19-21). “If, e.g., the read switch signal RS0 is activated to H level while data on the bit lines are amplified, data on the bit lines BL0n and /BL0n are transferred to the data lines DLn and /DLn (col. 5, lines 47-50).” “If, e.g., a write switch signal WS0 is activated, the transistors M12 to M15 are turned on to transfer data on the data lines DLn and /DLn to the bit lines BL0n and /BL0n, and write the data in the memory cell 35 (col. 5, lines 60-64).”

Yamada was relied upon by the Examiner to teach a sense amplifier circuit, but it shares the same deficiencies as Naritake by reading and writing data on the *same* pair of data lines Din, /Din (Fig. 6).

Applicant contends that neither Naritake, Yamada, nor their combination teaches or discloses each and every feature of the present invention as disclosed in independent claim 1. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

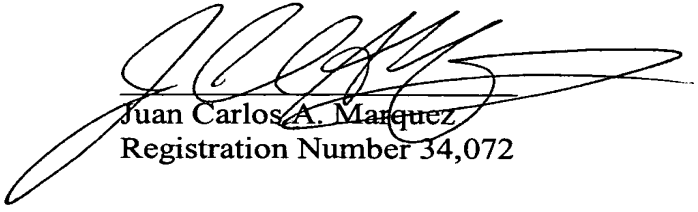
In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of

the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344



Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

January 21, 2005

SPF/JCM/JT